Process Control Limits in a CMOS ASIC Fabrication Process

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Abstract— *Converting GDSII input to a physical ASIC Device involves numerous process steps that require tight control to finally yield a device which can pass through thousands of test vectors successfully. To prevent or minimize the deviations from given specifications at various stages of wafer process, it is necessary that the process is under SPC.*

Conventional X and R charts developed for processes where only one source of variation exists; do not successfully predict the health of wafer fabrication processes where several independent sources of variation exist. The present paper describes a specific methodology suitable for wafer fabrication processes in arriving at Process Control Limits which indicate the health of the selected process and help in taking corrective actions as and when necessary. The paper deals with control limits for Run to Run variations.

Keywords— *Statistical Process Control, control limits, CMOS wafer fabrication*

I. INTRODUCTION

In a manufacturing industry, Statistical Process Control (SPC) helps in monitoring the production process and taking corrective action when the process goes out of control and thus helps in sustaining established product yields **[1]**. In an SPC method, statistics and statistical theories are applied on distributions and variations in distributions of measured parameters to arrive at process control limits. Walter Shewhart of Bell labs was the first person to develop the SPC tool in mid-1920. Since then the tool has become a major contributor in quality improvement process.

In a typical CMOS wafer fab, variations in transistor (functional) parameters such as threshold voltage, saturation current, breakdown voltage, leakage current, gain parameter etc. of a fabricated Application Specific Integrated Circuit (ASIC) may be caused due to changes in

a) Processes
b) Die location on wafer
c) Wafer position in the cassette
d) Time when the lot is processed
e) Equipment
f) Materials
g) Environment

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h) Operators
i) Inspections

Above changes may lead to following three main variations in measured parameters:

i. Within Wafer Variation (Based on location of measurement on single wafer)
ii. Wafer to Wafer Variation (Based on location of wafer in a cassette/ boat)
iii. Lot to Lot variation (Based on time when the lot is processed)

When all these variations fluctuate in expected manner, a stable pattern of many chance causes of variations develop. Chance causes are inevitable, undetectable and hence are to be ignored. Those causes of variation which are large in magnitude and hence readily identifiable are the assignable causes. When only chance causes are present in a process, process is said to be under control. However, when assignable causes also are present, variation will be excessive and process becomes out of control.

Thus measurement of parameters, statistical analysis of the data obtained and computation of control charts help in two ways – one in understanding the capability and accuracy within which process operates and the other in deciding whether the process is statistically under control or not in which case remedial action needs to be taken.

There are basically two types of control charts – average control chart (X-bar chart) and range control chart (R-chart). First one reveals how close the process is to the nominal design value and the latter reveals amount of spread (variability) around the nominal design value. The control chart has three lines – the upper control limit (UCL), Center Line (CL) and Lower Control Limit (LCL). These lines are computed from measurements on samples taken from production runs.

Often X–bar and R charts are developed for processes where only one source of variation exists. These are not of much help in a wafer fabrication process where multiple sources of variation, as indicated earlier, exist. These charts in fact mislead in such a way that even stable processes appear out of control and one keeps searching

frequently and frustratingly for non-existing assignable causes. Hence in a wafer fabrication process a different approach is needed in computing the Control Chart.

The present paper describes a specific methodology developed at SITAR to arrive at Process Control Limits for individual processes in the wafer fabrication. The paper demonstrates how presence of assignable causes can be detected from these control charts which in turn help in identifying the defective process that needs correction.

II. MATERIALS AND METHODS:

2.1. Details of Data

A typical one micron CMOS ASIC fabrication process is shown Fig 1. As indicated in the figure, standard fabrication of any ASIC - designed for SITAR fab involves total 13 masking steps

Fig 2 (a) shows SEM cross section of a typical CMOS device and Fig 2 (b) shows various layers in a pictorial representation.

Table 1 gives the quality parameters (Thickness) – specifications of different layers - that are to be measured and monitored in a typical production run. It is essential to measure and monitor these parameters routinely and use the data to verify whether the individual processes are in control or out of control.

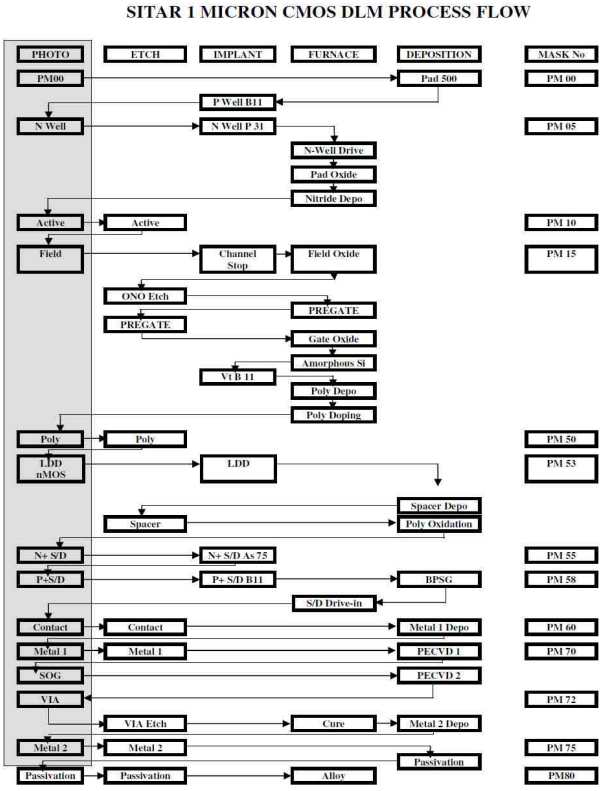

Fig 1: 1 Micron CMOS Process Flow

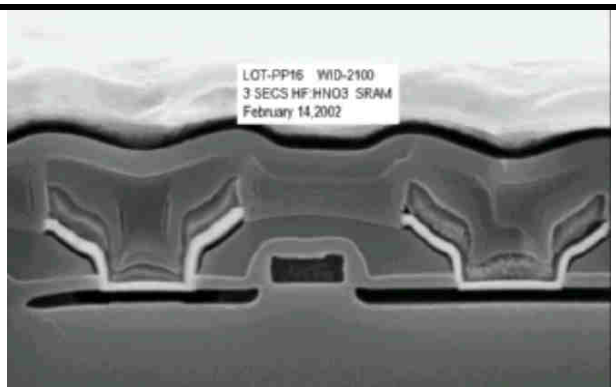

Fig 2 (a) SEM Cross Section of CMOS FET

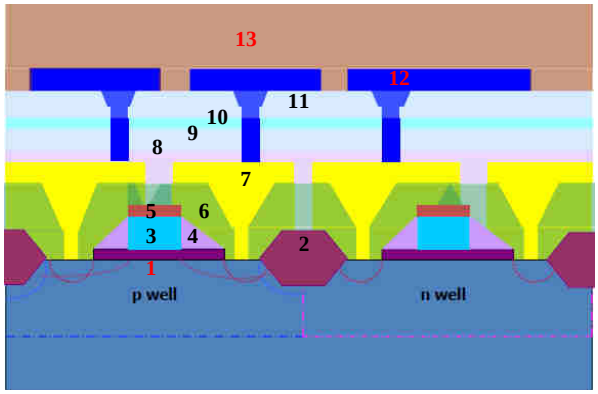

Fig 2 (b) Pictorial representation of CMOS FET

Following are the details of the layers as depicted in Fig 2 (b):

Layer	Description
1	Gate Oxide
2	Field Oxide
3	Polysilicon
4	Spacer Oxide
5	Polysilicon Oxide
6	Boro Phospho Silicate Glass
7	Metal 1: Aluminum
8 - 11	Inter Metallic Dielectric Stack
12	Metal 2: Aluminum
13	SION: SIilicon Oxy-Nitride

The data was collected from measurements over 10 lots, each lot consisting of 25 wafers. Wafers were of 6" dia with 12 µ thick 'p' epi layer (Resistivity: 8 – 12 Ω.cm) on 625 thick 'p+' bulk (Resistivity: 0.01-0.02 Ω.cm). Wafers were processed as per standard CMOS Fabrication technology (E10 –Twin Well DLM Process and LOCOS Device Isolation). Thickness measurements were made with KLA-Tencor ASET – F5 Model based on either DBS (Dual Beam Spectroscopy) or SE (Spectroscopic Ellipsometry) principle.

As a standard practice, the thickness for each process was measured at 9 locations on a wafer and on wafers taken from same slots of cassette in a run. Each cassette accommodates 25 wafers and the slots selected were 1, 5, 10, 15, 20 and 25.

Table 1: Quality Parameters – thickness of layers

Sl. No.	Description	Specification (In Å)
1	n-Well Drive In (Batch Process)	2400±60
2	Pad Oxide (Batch Process)	250±13
3	LPCVD Nitride (Batch Process)	1520±80
4	Field Oxide (Batch Process)	8500±200
5	Field Oxide after ONO (Single Wafer Process)	6900±300
6	Pre-Gate Oxide A (Batch Process)	225±15
7	Pre-Gate Oxide B (Batch Process)	6900±300
8	Pre-Gate Etch B (Single Wafer Process)	5600±300
9	Gate Oxide (Batch Process)	195±10
10	1st Polysilicon (Batch Process)	380±20
11	2nd Polysilicon (Batch Process)	4380±220
12	Spacer Oxide A (Batch Process)	2300±120
13	Spacer Oxide B (Batch Process)	7900±500
14	Polysilicon Oxide (Batch Process)	325±16
15	Boro Phospho Silicate Glass (Single Wafer Process)	7000±500
16	Contact etch – Wet (Single Wafer Process)	3000±300
17	PECVD Oxide 1(Single Wafer Process)	3000±125
18	Inter Metallic Dielectric Stack (Single Wafer Process)	8750±300
19	Via - Wet Etch (Single Wafer Process)	2000±300
20	SION : SIilicon Oxy-Nitide (Single Wafer Process)	15000±500

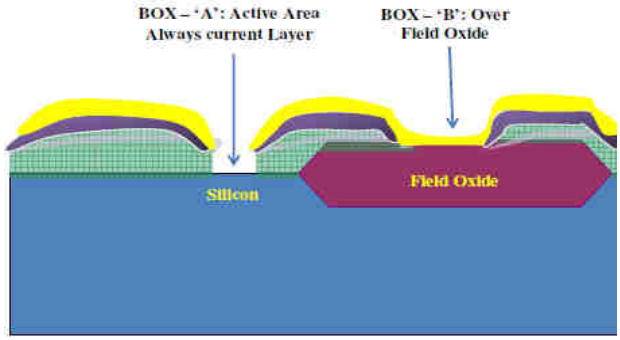

Fig 3: Measurement locations Box A and Box B

Thickness of a given layer under consideration was measured either at a location A/C on bare silicon (Often referred to as Box A measurement –Always current layer) or at a location B where the underneath layer would be oxide of silicon (Referred to as Box 'B' measurement – Over Field Oxide). The measurement locations are shown in Fig 3.

This data was initially used to arrive at the control limits. Subsequently data collected from about 18 to 20 lots were plotted to verify if the processes are in control or out of control.

2.2. Control chart computation methodology

In a typical wafer fabrication run, processes can be divided into two groups – one with single wafer process and the other a batch process as indicated in Table 1. In a single wafer process only within-wafer variations and run-to run variations exist. In a batch process, such as diffusion, wafer-to-wafer (within batch) variation also comes into picture due to for example a significant temperature differential from front to back in the furnace.

Effective control charts can be made based on data selection of rational sub-groups. In the present case the 9 specific locations selected on a wafer and six specific slots selected in a cassette, as described above, constitute the rational sub-group.

X-bar chart is computed as below:

- Step-1: X-Axis contains a subgroup number which identifies a particular sample consisting of a fixed number of observations. For example each sub-group is a wafer consisting 9 thickness measurements at 9 locations on the wafer.
- Step-2: Observations of sub-groups should be in same order for every wafer. First inspection gives first sub-group and last inspection gives last sub-group. For example slot 1 and slot 25 respectively in a cassette.
- Step-3: Y-axis is the variable – thickness in Å
- Step-4: Each point is the average of that sub-group i.e. mean of nine thickness values measured on the wafer.

- Step-5: Drawing the Central Line (CL). Average of averages – X double bar. x
- Step-6: Drawing UCL and LCL.
- UCL= X double bar + 3*MR bar/d_2 and LCL=X double bar – 3*MR bar/d_2
- d_2 is a constant depending on sample size. Since sample size for MR is 2, value of d_2 is taken as 1.128. **[2]**
- Control limits are frequently confused with spec limits which are permissible limits of a measurable quality parameter such as thickness.

MR-Chart (Moving Range Chart):

- Range is the difference between the biggest and smallest measured values. For example in a wafer out of the nine measurements made at nine locations the range is Thickness (Max) – Thickness (Min).
- The Central Line – CL is the average of all the sample ranges – R-bar
- UCL = D4*R-bar
- LCL = D3*R-bar
- D3 and D4 depend on sample size of each sample.
- D3 = 0, D4 = 3.267 [1]

III. RESULTS AND DISCUSSIONS

Following are X-double bar and MR charts for various quality parameters:

3.1. N-Well Drive-In (Thermal Process):

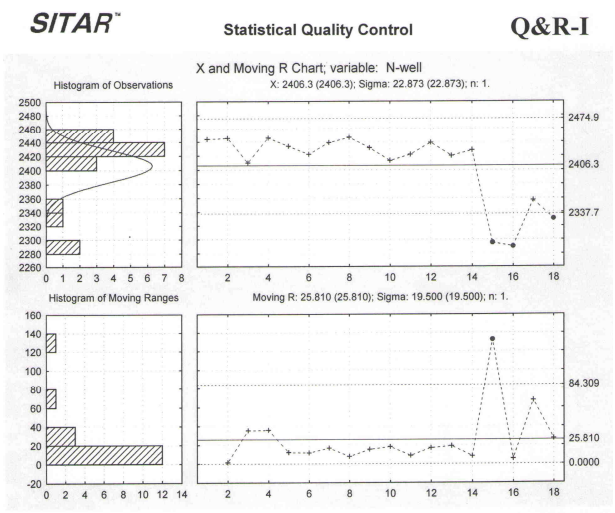

Fig 4: X double bar and MR Chart for N-Well Drive in

Fig 4 indicates that the N-well drive-in process had gone out of control subsequent to 14th lot and the concerned group had been informed for corrective action.

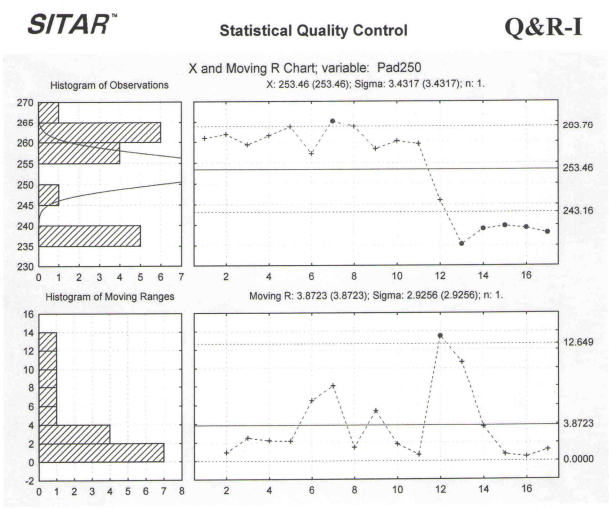

Fig 5: X double bar and MR Chart for Pad 250 Oxide

Fig 5 indicates that 250Å pad oxide realized through thermal oxidation was under control till 6th lot, after which the process went out of control. With subsequent corrective action the process could be brought under control till 12th lot. But once again the process went out of control. Corrective action is being taken to regain the control.

3.2. LPCVD Silicon Nitride deposition for active area:

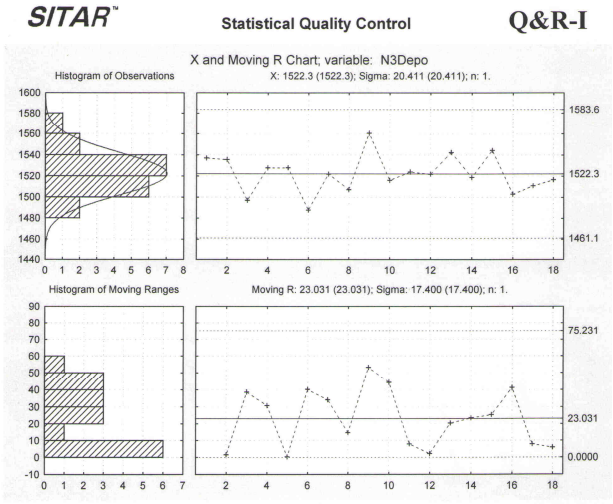

Fig 6: X double bar and MR Chart for Si_3N_4

Fig 6 indicates that the Silicon Nitride deposition through LPCVD was very much under control for all the lots.

3.3. Field Oxide through thermal oxidation for device isolation:

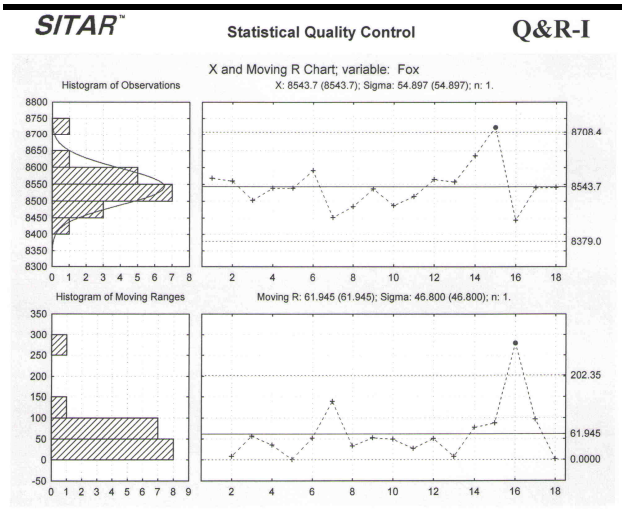

Fig 7: X double bar and MR Chart for Field Oxide

From Fig 7 it can be seen that the 8500Å field oxide realized through thermal oxidation was under control till 14th lot after which the process went out of control. With subsequent corrective action the process could be brought under control.

3.4. Oxide-Nitride-Oxide (ONO) wet etch:

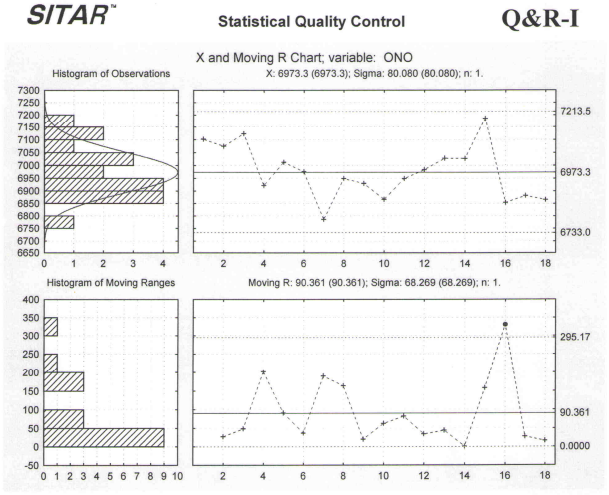

Fig 8: X double bar and MR Chart for Fox measurement after O-N-O etch

Fig 8 indicates that O-N-O etch was very much under control. However the range chart indicates that the spread in etched thickness for lot 16 had gone beyond control which could be brought back under control with corrective action.

3.5. Pre-Gate Oxide through thermal oxidation:

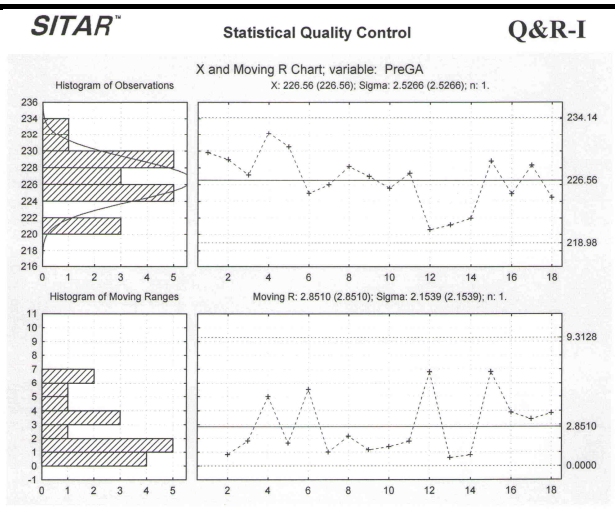

Fig 9: X double bar and MR Chart for Pre-gate Oxide Box-A measurement

Fig 9 and 10, thickness measured at Box A as well as Box B, clearly indicate that 225Å pre-gate oxide realized through thermal oxidation was very much under control.

3.6. Pre-Gate Oxide Etch:

Also, Fig 11, control chart for pre-gate oxide etch process as measured through the balance oxide at Box B indicates that the process was well under control.

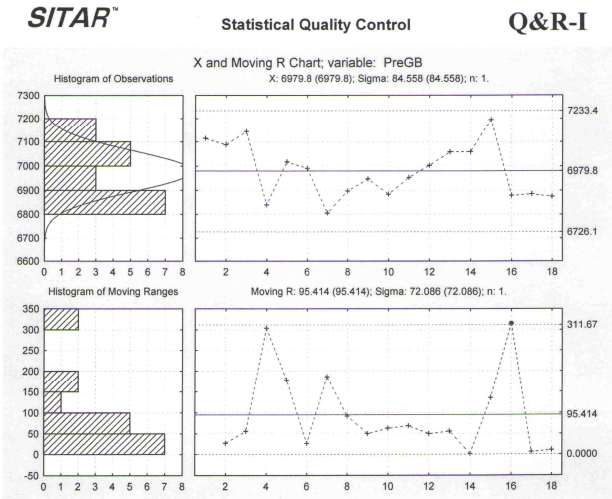

Fig 10: X double bar and MR Chart for Pre-gate Oxide Box-B measurement

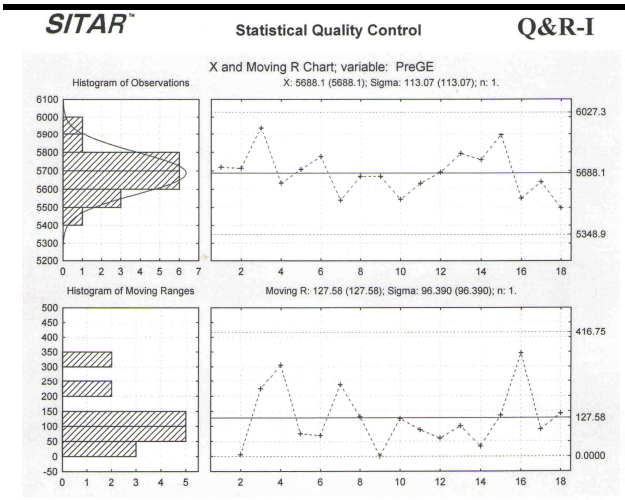

Fig 11: X double bar and MR Chart for Box-B measurement after pre-gate oxide etch

3.7. Gate Oxide through thermal oxidation:

Fig 12 and 13, control chart for Gate Oxide deposition as measured at Box A and Box B, was under control till lot 11. The deviations observed in lot 12 could be brought back within control limits subsequently.

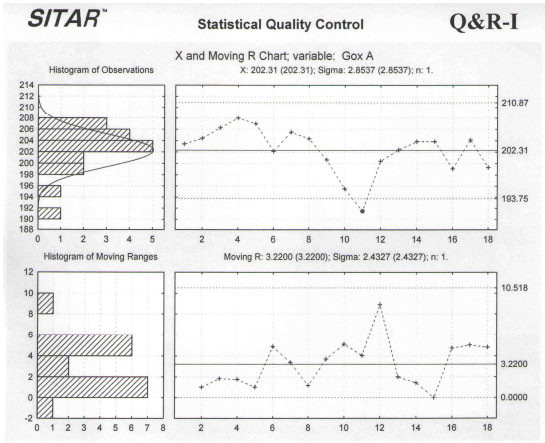

Fig 12: X double bar and MR Chart for Box-A measurement after Gate oxide deposition

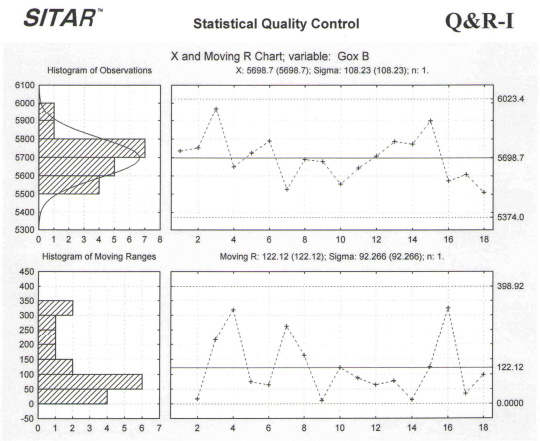

Fig 13: X double bar and MR Chart for Box-B measurement after Gate oxide deposition

3.8. Amorphous Silicon deposition through LPCVD:

Fig 14, control chart for amorphous silicon deposition through LPCVD indicates that the process was under control.

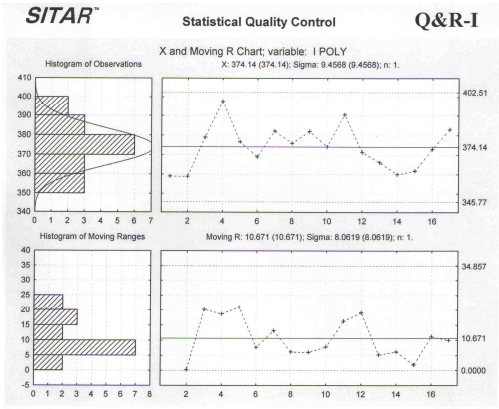

Fig 14: X double bar and MR Chart for Amorphous Silicon (First Poly)

3.9. Poly Silicon deposition through LPCVD for Gate contact:

Fig 15 reveals that the polysilicon deposition through LPCVD was under control till 15th lot. Later it went out of control and with corrective action the same could be brought under control in subsequent lots. Similarly as indicated in MR chart, the spread in deposition which went out of control for lot 16 could be brought back under control for subsequent lots.

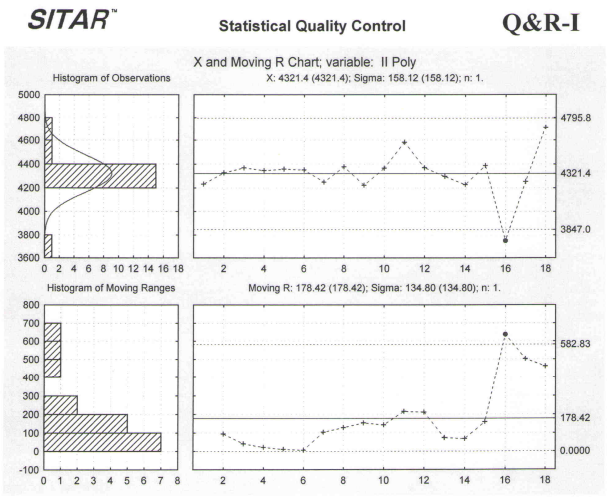

Fig 15: X double bar and MR Chart for Poly Silicon (Second Poly)

3.10. Spacer deposition through LPCVD for LDD Implant:

Fig 16 and 17, control charts for spacer oxide deposition as measured at Box A and Box B, indicate that the process was perfectly under control.

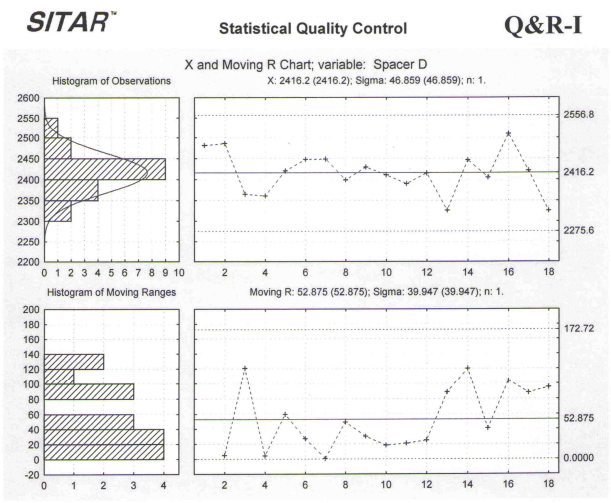

Fig 16: X double bar and MR Chart for Spacer Oxide at Box-A

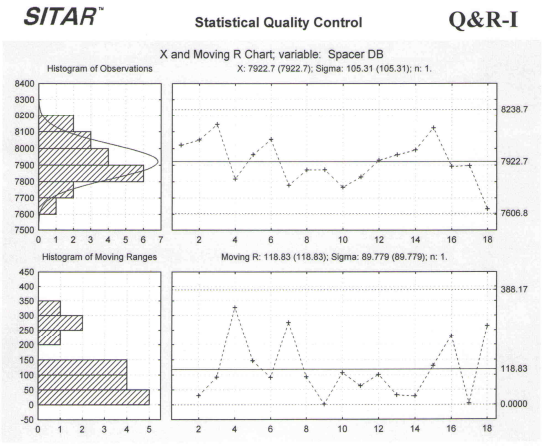

Fig 17: X double bar and MR Chart for Spacer Oxide at Box-B

3.11. Spacer etch:

Fig 18, control chart for spacer oxide etch as measured at Box B, indicates that the process was perfectly under control.

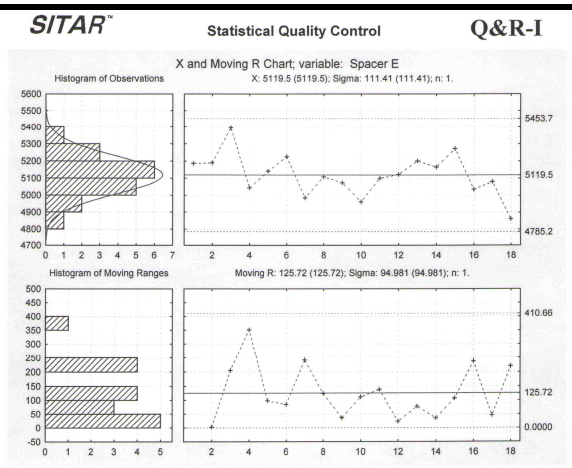

Fig 18: X double bar and MR Chart at Box-B after Spacer Oxide etch

3.12. Poly Oxidation:

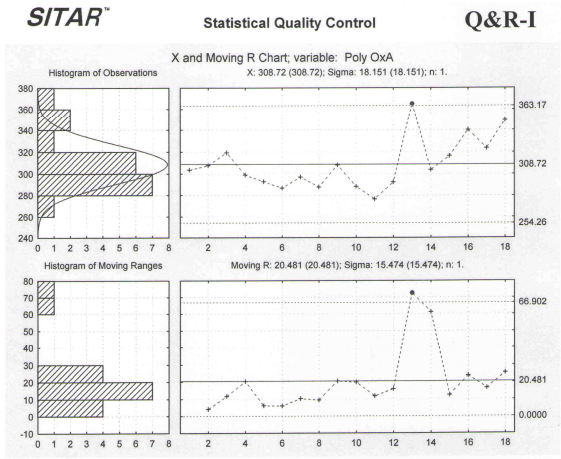

Fig 19: X double bar and MR Chart at Box-A after Poly Oxidation

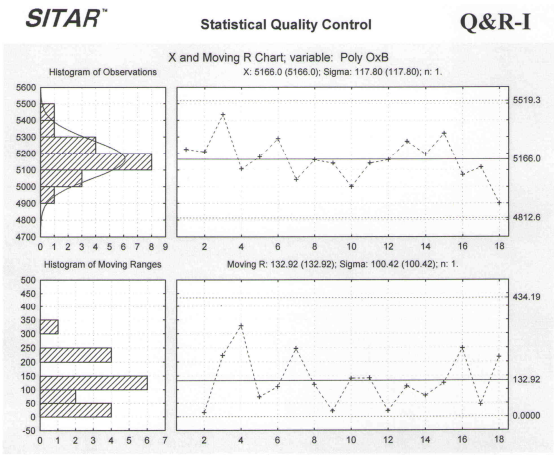

Fig 20: X double bar and MR Chart at Box-B after Poly Oxidation

Fig 19 and 20 control charts for poly oxidation at box A and B respectively. Fig 19 indicates that the process which went out of control for lot 13 could be brought back under control for subsequent lots. The out of control situation was not reflected in Box B measurement since the increase

due to poly oxidation was small compared to large FOX thickness below.

3.13. Boro Phospho Silicate Glass (BPSG) deposition through PECVD:

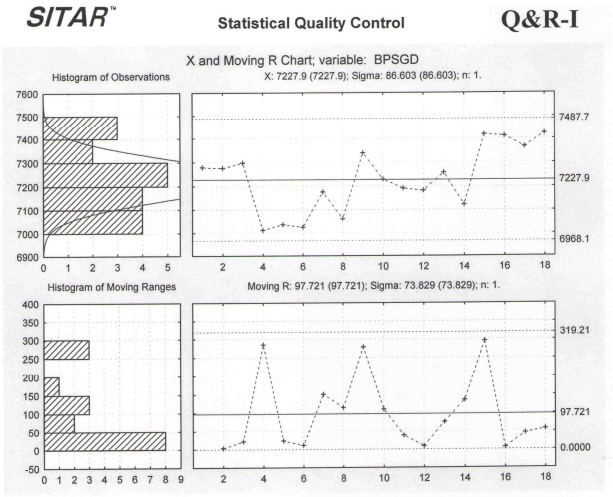

Fig 21: X double bar and MR Chart for BPSG Deposition at Box-A

Fig 21and 22 for BPSG deposition at box A and B respectively indicate that the process was under control.

3.14. Contact window etch in BPSG Wet etch:

Fig 23 and 24 for contact wet etch in BPSG as measured at Box A and B respectively. Fig 23 indicates that the process went out of control for lot 15 which could be successfully brought under control with appropriate
corrective action in the process recipe.

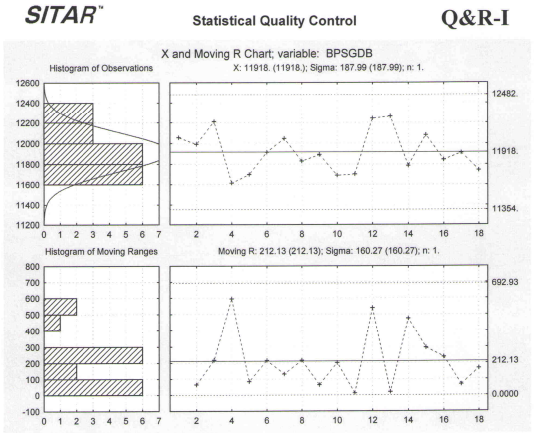

Fig 22: X double bar and MR Chart for BPSG Deposition at Box-B

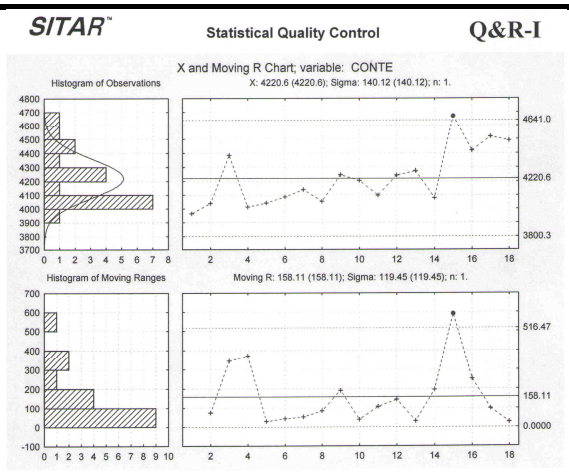

Fig 23: X double bar and MR Chart at Box A after contact window wet etch in BPSG

However the out of control situation for wet etch was not reflected in Box B measurement for the same reasons mentioned earlier.

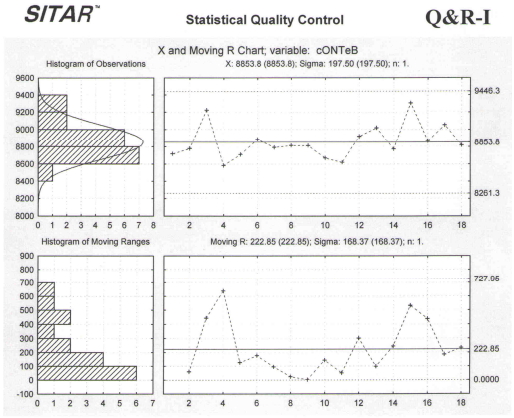

Fig 24: X double bar and MR Chart at Box B after contact window wet etch in BPSG

3.15. Contact window etch in BPSG Dry etch:

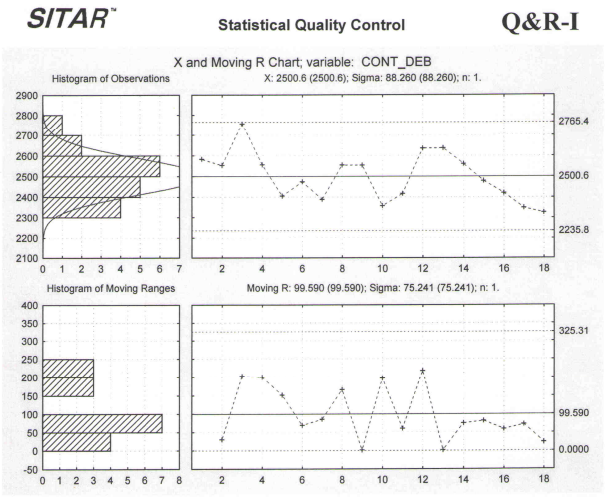

Fig 25: X double bar and MR Chart at Box B after contact window Dry etch in BPSG

Fig 25 reveals that the contact dry etch in BPSG as measured at Box B was well under control

3.16. Metal -1 etch:

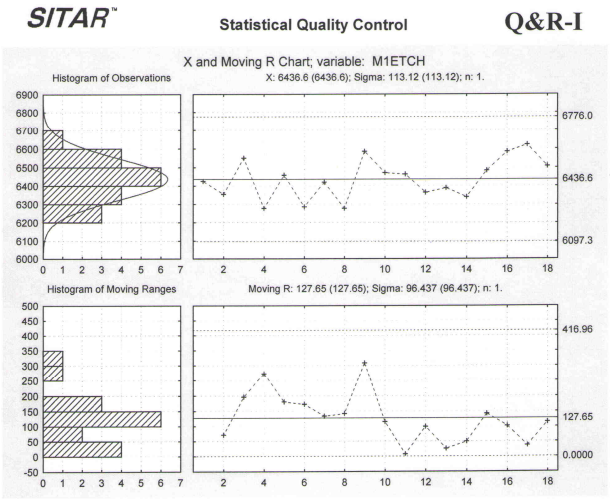

Fig 26: X double bar and MR Chart at Box B after Metal-1 etch

It is evident from Fig 26 - the control chart for metal etch, that the process as measured at Box B was well under control.

3.17. First Inter Metallic Dielectric (IMD) deposition through PECVD for Metal-1 and Metal-2 isolation:

Fig 27 and 28 are control charts for IMD1 deposition as measured at Box A and Box C respectively. Box A and Box C are identical till BPSG deposition. When BPSG is etched, BPSG remains in Box C, while it gets etched in Box A. As indicated in Fig 27 and 28, the IMD1 deposition process was in control till 17th lot and had become out of control for 18th lot. Corrective action was initiated to bring back the process under control.

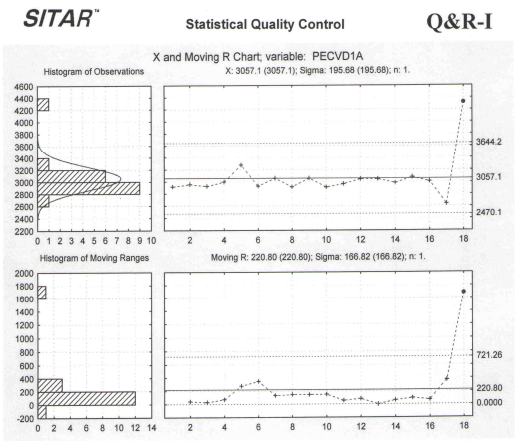

Fig 27: X double bar and MR Chart at Box-A after First PECVD deposition

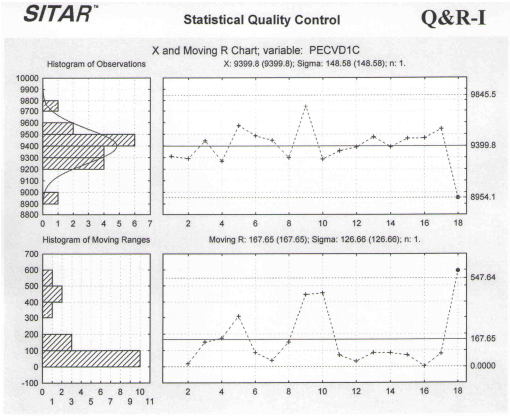

Fig 28: X double bar and MR Chart at Box-C after First PECVD deposition

3.18. Second Inter Metallic Dielectric (IMD) deposition:

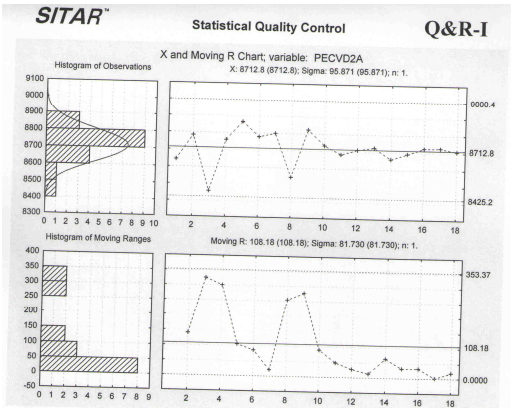

Fig 29: X double bar and MR Chart at Box-A after PECVD stack deposition

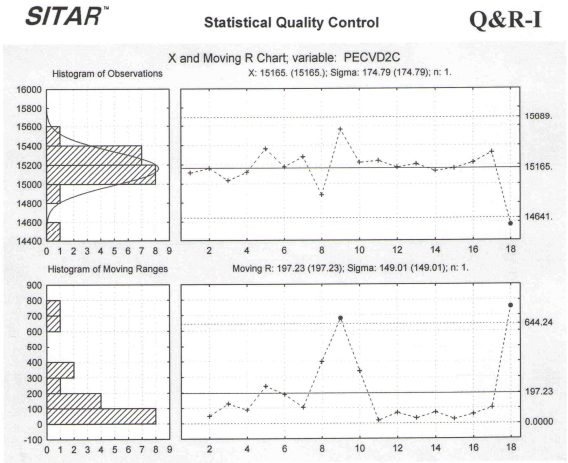

Fig 30: X double bar and MR Chart at Box-C after PECVD stack deposition

It is evident from Fig 29 and 30 - the control charts for PECVD Oxide1/SOG (Spin –On-Glass)/PECVD Oxide2

stack, that the process, as measured at Box A and Box C respectively, was well under control till lot 17. The process went out of control for lot 18 based on which need for corrective action was communicated to the respective process group.

3.19. Via etch - Wet in IMD Stack for Metal 1 and Metal 2 Interconnection:

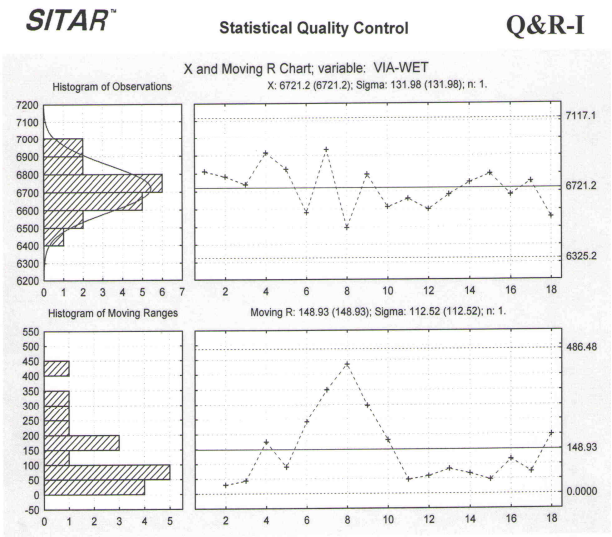

Fig 31: X double bar and MR Chart at Box-A after VIA-Wet Etch

Fig 31 and 32 are the control charts for via wet etch in IMD Stack as measured at Box A and Box C respectively. The figures indicate that the process was well under control till lot 17. The process went out of control for lot 18, based on which corrective action was initiated.

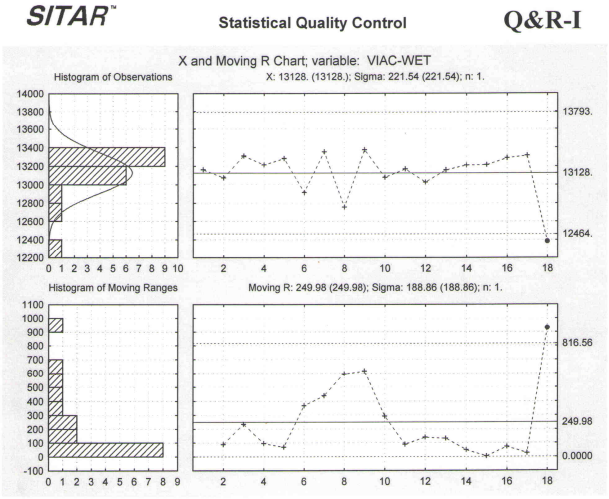

Fig 32: X double bar and MR Chart at Box-C after VIA-Wet Etch

3.20. Via etch - Dry in IMD Stack for Metal 1 and Metal 2 Interconnection:

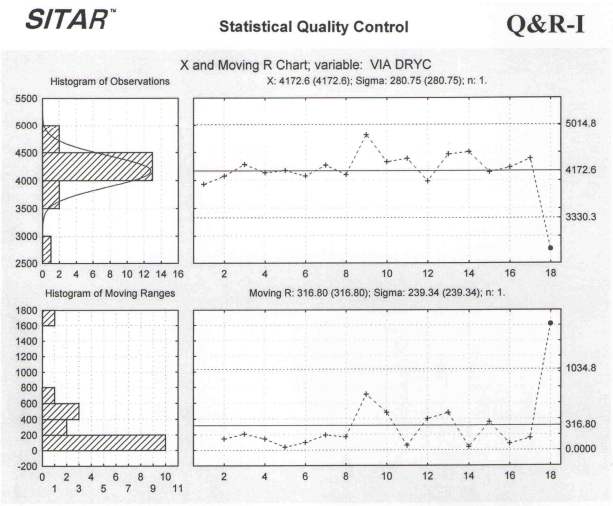

Fig 33: X double bar and MR Chart at Box-C after VIA-Dry Etch

Fig 33 - the control charts for dry etch of IMD stack as measured at Box C. It is evident from the figure that the dry etch process for via was well under control till lot 17and went out of control for lot 18. Accordingly corrective action was suggested.

3.21. Final Passivation – deposition of Silicon Oxy-Nitride through PECVD:

Fig 34 - the control chart for final passivation i.e. thickness of silicon oxy nitride as measured on metal 2 pad was well under control till lot 17and went out of control for lot 18. Accordingly corrective action was suggested.

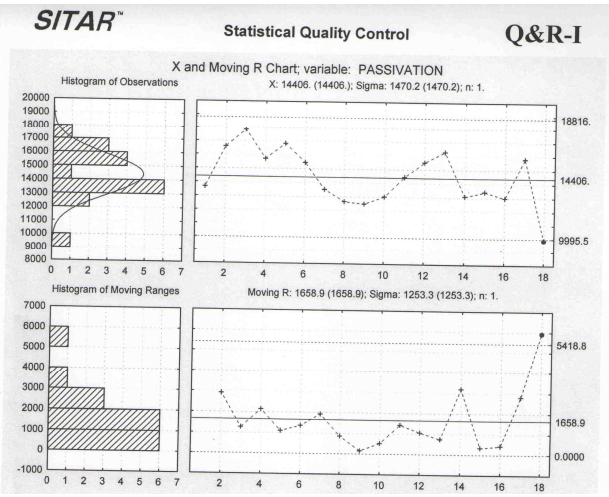

Fig 34: X double bar and MR Chart for Passivation

IV. CONCLUSIONS

The health of a wafer fabrication process can be successfully monitored with SPC tools such as control

charts for measured quality parameters. However a wafer fab such as a one-micron CMOS ASIC fab needs a slightly different methodology to arrive at the control limits especially to know run-to run (lot to lot) drifts in processes. Once the control limits are established, it becomes easy to detect out of control situations and take immediate corrective actions.

ACKNOWLEDGEMENTS

The authors are thankful to Dr.A.Linga Murthy, CEO, SITAR for his encouragement in carrying out this work.

Authors are also thankful to process and character-rization groups for wafer processing and providing the required data.

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